

# DATA SHEET

## **CBTS3306**

Dual bus switch with Schottky diode clamping

Product data

2001 Nov 08

File under Integrated Circuits — ICL03

# Dual bus switch with Schottky diode clamping

CBTS3306

## FEATURES

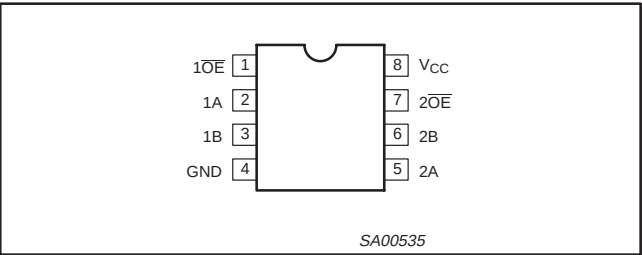
- 5  $\Omega$  switch connection between two ports
- TTL-compatible input levels
- Package options include plastic small outline (SO) and thin shrink small outline (TSSOP)
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

## DESCRIPTION

The CBTS3306 Dual FET Bus Switch features independent line switches with Schottky diodes on the I/Os to clamp undershoot. Each switch is disabled with the associated Output Enable ( $\overline{OE}$ ) input is high.

The CBTS3306 is characterized for operation from  $-40$  to  $+85$   $^{\circ}\text{C}$ .

## PIN CONFIGURATION



## PIN DESCRIPTION

| PIN NUMBER | SYMBOL                              | NAME AND FUNCTION       |
|------------|-------------------------------------|-------------------------|
| 1, 7       | $1\overline{OE}$ , $2\overline{OE}$ | Output enable           |
| 2, 5       | 1A, 2A                              | A port inputs           |
| 3, 6       | 1B, 2B                              | B port outputs          |
| 4          | GND                                 | Ground (0 V)            |
| 8          | $V_{CC}$                            | Positive supply voltage |

## QUICK REFERENCE DATA

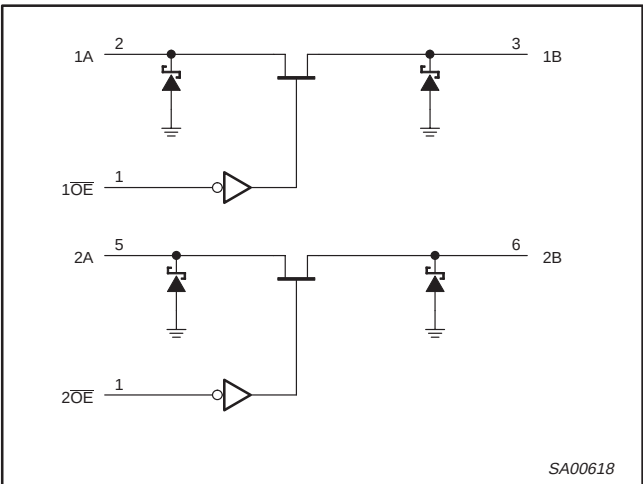
| SYMBOL                 | PARAMETER                             | CONDITIONS<br>$T_{amb} = 25$ $^{\circ}\text{C}$ ; GND = 0 V | TYPICAL    | UNIT          |
|------------------------|---------------------------------------|-------------------------------------------------------------|------------|---------------|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>A to B or B to A | $C_L = 50$ pF; $V_{CC} = +5.0$ V $\pm 0.5$ V                | 0.25 (MAX) | ns            |
| $C_{IO(OFF)}$          | Port off capacitance                  | $V_O = 3$ V or 0; $\overline{OE} = V_{CC}$                  | 7.60       | pF            |
| $I_{CC}$               | Quiescent supply current              | $V_{CC} = 5.5$ V; $I_O = 0$ , $V_I = V_{CC}$ or GND         | 3          | $\mu\text{A}$ |

## ORDERING INFORMATION

| PACKAGES            | TEMPERATURE RANGE                | ORDER CODE | DWG NUMBER |
|---------------------|----------------------------------|------------|------------|
| 8-pin plastic SO    | $-40$ to $85$ $^{\circ}\text{C}$ | CBTS3306D  | SOT96-1    |
| 8-pin plastic TSSOP | $-40$ to $85$ $^{\circ}\text{C}$ | CBTS3306PW | SOT530-1   |

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

## LOGIC DIAGRAM (positive logic)



## FUNCTION TABLE

| INPUT           | FUNCTION        |
|-----------------|-----------------|
| $\overline{OE}$ |                 |
| L               | A port = B port |
| H               | Disconnect      |

## Dual bus switch with Schottky diode clamping

CBTS3306

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>** $T_{amb} = -40$  to  $+85$  °C, unless otherwise specified.

| SYMBOL    | PARAMETER                     | CONDITIONS   | RATING       | UNIT |
|-----------|-------------------------------|--------------|--------------|------|
| $V_{CC}$  | DC supply voltage             |              | -0.5 to +7.0 | V    |
| $V_I$     | DC input voltage <sup>2</sup> |              | -0.5 to +7.0 | V    |
| $I_{OUT}$ | DC output current             |              | 128          | mA   |
| $I_{IK}$  | Diode current                 | $V_{IO} < 0$ | -50          | mA   |
| $T_{stg}$ | Storage temperature range     |              | -65 to +150  | °C   |

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51.

**RECOMMENDED OPERATING CONDITIONS<sup>1</sup>**

| SYMBOL    | PARAMETER                            | LIMITS |     | UNIT |
|-----------|--------------------------------------|--------|-----|------|
|           |                                      | MIN    | MAX |      |
| $V_{CC}$  | DC supply voltage                    | 4.5    | 5.5 | V    |
| $V_{IH}$  | High-level input voltage             | 2.0    | —   | V    |
| $V_{IL}$  | Low-level Input voltage              | —      | 0.8 | V    |
| $T_{amb}$ | Operating free-air temperature range | -40    | +85 | °C   |

**NOTE:**

- All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

**DC ELECTRICAL CHARACTERISTICS** $T_{amb} = -40$  to  $+85$  °C, unless otherwise specified.

| SYMBOL                       | PARAMETER                                            |                | TEST CONDITIONS                                                                      | LIMITS                           |                  |      | UNIT |
|------------------------------|------------------------------------------------------|----------------|--------------------------------------------------------------------------------------|----------------------------------|------------------|------|------|
|                              |                                                      |                |                                                                                      | T <sub>amb</sub> = −40 to +85 °C |                  |      |      |
|                              |                                                      |                |                                                                                      | MIN                              | TYP <sup>1</sup> | MAX  |      |
| V <sub>IK</sub>              | Input clamp voltage                                  | A or B input   | V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA                                     | —                                | —                | −0.7 | V    |
|                              |                                                      | Control inputs | V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA                                     | —                                | —                | −1.2 |      |
| I <sub>I</sub>               | Input leakage current                                |                | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V                               | —                                | —                | ±1   | μA   |
| I <sub>CC</sub>              | Quiescent supply current                             |                | V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | —                                | —                | 3    | μA   |
| V <sub>P</sub>               | Output high pass voltage                             |                | V <sub>O</sub> = V <sub>CC</sub> = 5.0 V; I <sub>I</sub> = −100 mA                   | 3.4                              | 3.6              | 3.9  | V    |
| ΔI <sub>CC</sub>             | Additional supply current per input pin <sup>2</sup> |                | V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND  | —                                | —                | 2.5  | mA   |
| C <sub>I</sub>               | Control pin capacitance                              |                | V <sub>I</sub> = 3 V or 0                                                            | —                                | 3.25             | —    | pF   |
| C <sub>IO(OFF)</sub>         | Port off capacitance                                 |                | V <sub>O</sub> = 3 V or 0; $\overline{OE}$ = V <sub>CC</sub>                         | —                                | 7.60             | —    | pF   |
| r <sub>on</sub> <sup>3</sup> | On-resistance                                        |                | V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA                | —                                | 3.4              | 5    | Ω    |
|                              |                                                      |                | V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA                | —                                | 3.4              | 5    | Ω    |
|                              |                                                      |                | V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = 15 mA              | —                                | 6.8              | 7.5  | Ω    |

**NOTES:**

- All typical values are at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C.
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

Dual bus switch with Schottky diode clamping

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AC CHARACTERISTICS

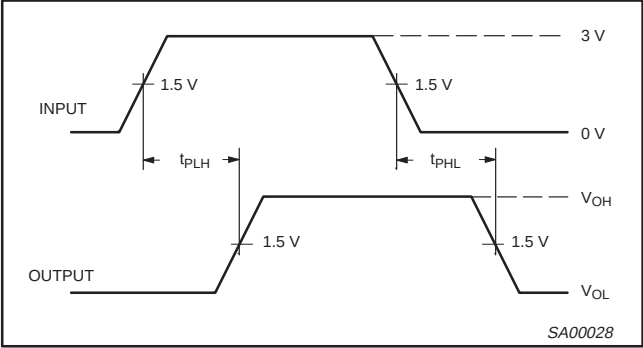
T<sub>amb</sub> = −40 to +85 °C; C<sub>L</sub> = 50 pF

| SYMBOL           | PARAMETER                                   | FROM (INPUT)           | TO (OUTPUT) | LIMITS                          |      | UNIT |
|------------------|---------------------------------------------|------------------------|-------------|---------------------------------|------|------|
|                  |                                             |                        |             | V <sub>CC</sub> = +5.0 V ±0.5 V |      |      |
|                  |                                             |                        |             | MIN                             | MAX  |      |
| t <sub>pd</sub>  | Propagation delay <sup>1</sup>              | A or B                 | B or A      | —                               | 0.25 | ns   |
| t <sub>en</sub>  | Output enable time to High and Low level    | $\overline{\text{OE}}$ | A or B      | 1.8                             | 5    | ns   |
| t <sub>dis</sub> | Output disable time from High and Low level | $\overline{\text{OE}}$ | A or B      | 1                               | 5    | ns   |

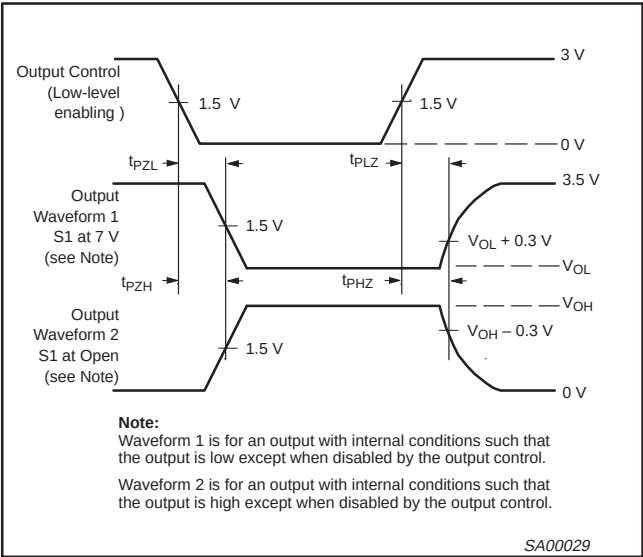
**NOTE:**  
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V<sub>M</sub> = 1.5 V, V<sub>IN</sub> = GND to 3.0 V



Waveform 1. Input to Output Propagation Delays

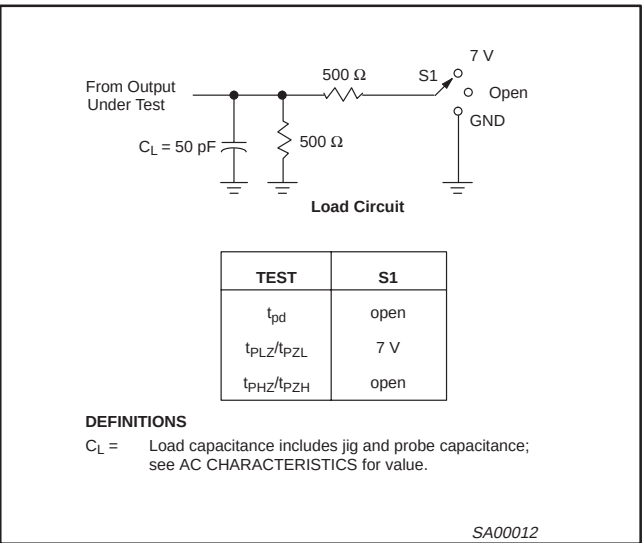


**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

- NOTES:**
- t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

TEST CIRCUIT AND WAVEFORMS



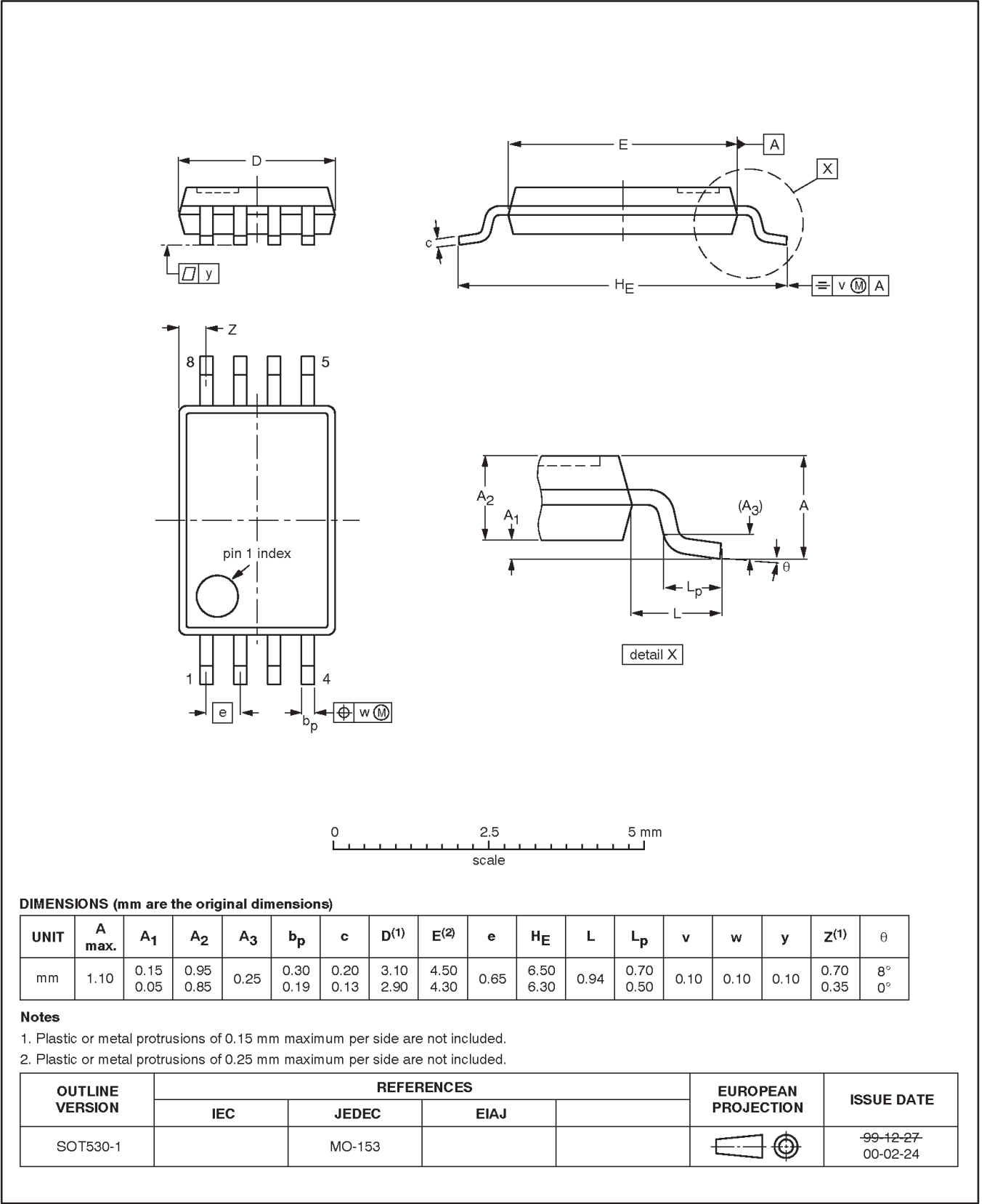
- NOTES:**
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.

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TSSOP8: plastic thin shrink small outline; 8 leads; body width 4.4 mm

SOT530-1

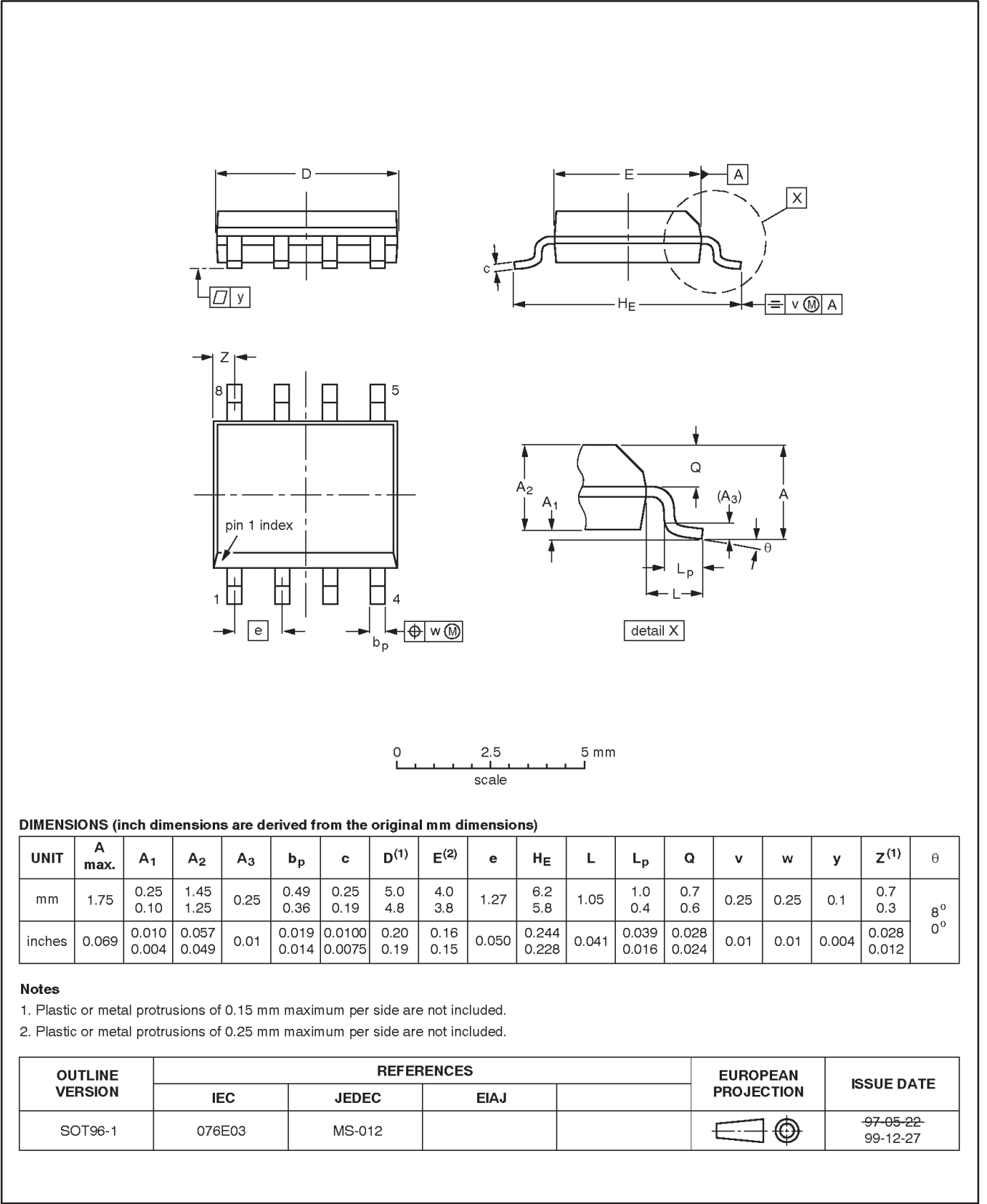


Dual bus switch with Schottky diode clamping

CBTS3306

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



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Dual bus switch with Schottky diode clamping

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**NOTES**

## Dual bus switch with Schottky diode clamping

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## Data sheet status

| Data sheet status <sup>[1]</sup> | Product status <sup>[2]</sup> | Definitions                                                                                                                                                                                                                                                                                                            |
|----------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                                            |
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